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05/03/02

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PATENT NUMBER and  
ISS 6596568



6596568

U.S. UTILITY Patent Application

APPL. NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10053572	05/03/2002	438	08	2812	

\*\*APPLICANTS: Hsu Chi-Hsing;

\*\*CONTINUING DATA VERIFIED:

\*\* FOREIGN APPLICATIONS VERIFIED:

TAIWAN 90132737 12/28/2001

PG-PUB DO NOT PUBLISH ☐

RESCIND ☐

Foreign priority claimed

☒ yes ☐ no

35 USC 119 conditions met

☒ yes ☐ no

ATTORNEY DOCKET NO

Verified and Acknowledged Examiners's initials

8289-US-PA

TITLE: Wafer level packaging and chip structure

U.S. DEPT. OF COMM./PAT. & TM-PTO-438L (Rev. 12-01)

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6/19/03

Formal Drawings (7 sheets) set L

5/13/02

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
3- 12-03		Total Claims 16	Print Claim for O.G. 1
ISSUE FEE <input checked="" type="checkbox"/>		DRAWING	
Amount Due \$1600	Date Paid 5-28-03	Sheets Drwg. 7	Figs. Drwg. 13
<input type="checkbox"/> TERMINAL DISCLAIMER		Print Fig. 9	Application Examiner Theresa Shind
PREPARED FOR ISSUE		WARNING: The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368, Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.	

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